

	Application No.	Applicant(s)
A	10/620,698	WATANABE ET AL.
Notice of Allowability	Examiner	Art Unit
	Andy Huynh	2818
The MAILING DATE of this communication app All claims being allowable, PROSECUTION ON THE MERITS IS herewith (or previously mailed), a Notice of Allowance (PTOL-85) NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT R of the Office or upon petition by the applicant. See 37 CFR 1.313	(OR REMAINS) CLOSED in this or other appropriate communica IGHTS. This application is subje	application. If not included atton will be mailed in due course. THIS
1. $igspace$ This communication is responsive to <u>the Amendment date</u>	<u>d 12/22/2004</u> .	
2. \boxtimes The allowed claim(s) is/are <u>1,2,4-12 and 16-32</u> .		
3. $igotimes$ The drawings filed on <u>22 December 2004</u> are accepted by	the Examiner.	
 4. Acknowledgment is made of a claim for foreign priority ur a) All b) Some* c) None of the: 1. Certified copies of the priority documents have 2. Certified copies of the priority documents have 3. Copies of the certified copies of the priority do International Bureau (PCT Rule 17.2(a)). * Certified copies not received: 	e been received. e been received in Application No)
Applicant has THREE MONTHS FROM THE "MAILING DATE" noted below. Failure to timely comply will result in ABANDONN THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.		ply complying with the requirements
5. A SUBSTITUTE OATH OR DECLARATION must be subm INFORMAL PATENT APPLICATION (PTO-152) which give		
6. CORRECTED DRAWINGS (as "replacement sheets") mus (a) including changes required by the Notice of Draftspers 1) hereto or 2) to Paper No./Mail Date (b) including changes required by the attached Examiner' Paper No./Mail Date Identifying indicia such as the application number (see 37 CFR 1 each sheet. Replacement sheet(s) should be labeled as such in the	son's Patent Drawing Review (P . s Amendment / Comment or in the dr .84(c)) should be written on the dr	ne Office action of awings in the front (not the back) of
 DEPOSIT OF and/or INFORMATION about the depo attached Examiner's comment regarding REQUIREMENT 		
Attachment(s) 1. ☐ Notice of References Cited (PTO-892)		al Patent Application (PTO-152)
2. Notice of Draftperson's Patent Drawing Review (PTO-948)	6. ☐ Interview Summ Paper No./Mail	ary (PTO-413), Date
 Information Disclosure Statements (PTO-1449 or PTO/SB/C Paper No./Mail Date 	08), 7. ⊠ Examiner's Ame	endment/Comment
4. Examiner's Comment Regarding Requirement for Deposit	8. 🛛 Examiner's State	ement of Reasons for Allowance
of Biological Material	9. Other	
<u> </u>	and	1. Muno
	Pat	ent Examiner
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DETAILED ACTION

In the Amendment dated December 22, 2004, Figs. 21-22 of the drawings are amended, claims 3 and 13-15 are canceled, claims 1, 10, 12, 16 and 17 are amended, and new claims 27-32 are added. Accordingly, claims 1-2, 4-12 and 16-32 are currently pending in this application.

Examiner's Amendment

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

In claim 16, "The device according to claim 14" is changed to – The device according to claim 12--, due to claim 14 is canceled.

In claim 17, line 12, "... a <u>ate</u> insulating film ..." is changed to -... a <u>gate</u> insulating film ...-, and in claim 28, line 3, "first ate" is changed to -first gate--.

Allowable Subject Matter

Claims 1-2, 4-12 and 16-32 are allowed.

The following is an examiner's statement of reason for allowance:

Claims 1, 2, 4-9 and 31 are allowable over the prior art of record because the prior art of record does not teach or render obvious a semiconductor device comprises, in combination with all other features, a first lower electrode provided on the second impurity diffusion area, and in

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addition, a first contact plug partly provided in the first trench and electrically connecting the first interconnection layer and the first impurity diffusion area as recited in independent claim 1.

Claims 10 and 11 are allowable over the prior art of record because the prior art of record does not teach or render obvious a semiconductor device comprises, in combination with all other features, a first lower electrode provided on the second impurity diffusion area, and in addition, a first insulating film covering the first gate electrode and a second insulating film which is buried in the first trench and different from the first insulating film as recited in independent claim 10.

Claims 12, 16 and 32 are allowable over the prior art of record because the prior art of record does not teach or render obvious a semiconductor memory device comprises, in combination with all other features, each capacitor comprising a lower electrode provided on the second impurity diffusion area, and in addition, each of the plurality of first contact plugs is partly provided in one of the plurality of trenches and electrically connects one of the plurality of the interconnection layers and the first impurity diffusion area as recited in independent claim 12.

Claims 17, 18 and 30 are allowable over the prior art of record because the prior art of record does not teach or render obvious a semiconductor device comprises, in combination with all other features, a first lower electrode provided on the second impurity diffusion area, and in addition, a first insulating film covering the first gate electrode and a second insulating film which is buried in the first trench and different from the first insulating film as recited in independent claim 17.

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Claims 19-22 are allowable over the prior art of record because the prior art of record does not teach or render obvious a method of manufacturing a semiconductor memory device comprises, in combination with all other features, forming a lower electrode on the second impurity diffusion area as recited in independent claim 19.

Claims 23-26 are allowable over the prior art of record because the prior art of record does not teach or render obvious a method of manufacturing a semiconductor memory device comprises, in combination with all other features, forming lower electrodes on each of the second impurity diffusion areas as recited in independent claim 23.

Claims 27-29 are allowable over the prior art of record because the prior art of record does not teach or render obvious a semiconductor memory device comprises, in combination with all other features, a first lower electrode provided on the second impurity diffusion area, and a second lower electrode provided on the third impurity diffusion area as recited in independent claim 27.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance".

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Conclusion

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy Huynh whose telephone number is (571) 272-1781. The

examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, David Nelms can be reached on (571) 272-1787. The fax phone numbers for the

organization where this application or proceeding is assigned are (703) 872-9306 for regular

communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding

should be directed to the receptionist whose telephone number is (703) 308-0956.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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02/02/05

Andy Huynh

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Patent Examiner